VBFO (638-6067-001)

Rockwell International

instructions

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1. DESCRIPTION

VBFO 638-6067-001, shown in figure 1, is a 2-layer planar card with a 56-pin edge-on connector (2 layers, 28 pins each) and two subminiax rf connectors.

The VBFO consists of a synthesized bfo, a bcd up/-down counter, an end-stop circuit, and a polarity change control circuit.

2. PRINCIPLES OF OPERATION

2.1 General

The vbfo receives the following inputs:

a. 450-kHz reference
b. Preset vbfo (parallel bcd) input or vbfo tune input
c. Vbfo/450-kHz switching inputs
d. Necessary associated control signals to activate and control the vbfo output frequency.

The vbfo produces the following outputs:

a. A bfo offset if frequency output (440.01 to 459.99 kHz in 10-Hz steps)
b. A parallel bcd output for displays

The vbfo circuits are enabled by a vbfo enable signal (logic 1) at P1-46. The vbfo/450-kHz control enables the vco, output switching, and the phase/frequency discriminator. Refer to figure 2.

2.2 Synthesized BFO

A 450-kHz reference input signal at J2 is applied through buffer circuit Q16 and is divided by 1500 (by fixed dividers U38, U39, and U33) to produce 300-Hz reference frequency signals that are applied to sampling gates U9A, U9B, U9C, and U9D, in the voltage-controlled oscillator (vco), through sampling logic circuits U34, Q4, and Q5.

(To Be Supplied)

VBFO
Figure 1

Decade counters U19, U24, U27, U31, and U32 form a programmable frequency divider with variable division ratios ranging from 44 001 to 45 999, with 45 000 the division ratio for 0 vbfo offset from the selected operating frequency. The division ratios for the various vbfo settings are determined by the bcd frequency information from the preset vbfo (parallel bcd) input or parallel bcd output for the bcd up/down counter. The +/- signal is determined by the +/- input signal and by up/down and reset logic circuit U13, U14, and the vbfo polarity change circuit. The output of the programmable divider circuit is applied through the phase/frequency discriminator and then to the sampling gates in the vco assembly.

The vco assembly generates an output frequency that ranges from 13.2003 to 13.7997 MHz with 13.5000 MHz as the center frequency (0 vbfo offset). The output from the vco assembly is used as the clock signal for the programmable divider circuit and is divided by 30 (by fixed divider circuits U3 and U1) to become the vbfo output signal that ranges from 440.01 to 459.99 kHz.

The division ratio of the programmable dividers is accomplished by loading 45 000 into the counters, adding the vbfo offset frequency, and then allowing the counters to count down to 00 000. Assume that the BFO is set to the maximum deviation, 9.990 kHz, above the operating frequency. The +/- input goes to + (logic 1), which causes the up/down and reset logic circuit to set the programmable divider circuit to the required 45 000 division ratio and to a countdown state. The 999 input from the bcd frequency input is loaded, making a total division ratio of 45 999 (the countdown starting point). The counter circuit then divides by counting down to 00 000. The clock input to the divider circuit, at this point, will be different from the required 13.7997 MHz (depending upon the previous vbfo offset frequency), which causes the output of the counter circuit applied to the sampling gates to be less than the 300-Hz nominal frequency. The sampling gates in the vco assembly function basically as a phase comparator. The 300-Hz control inputs, produced from the 450-kHz reference input, enable the gates at the 300-Hz control (logic 0) pulse rate. If the input signal from the programmable divider is out of phase, the out-of-phase portion of the signal is passed through the gates during the enable period. The more out of phase the input signal, the greater the amplitude of the output signal from the gates. The output of the gates is filtered and amplified by capacitor C29 and FET Q8 to produce a dc error voltage. The dc error voltage is applied across voltage variable capacitance diode VR4. As the voltage across VR4 increases, its capacitance decreases, thus increasing the frequency of the voltage-controlled oscillator circuit (U4). Conversely, as the dc error voltage across VR4 decreases, the capacitance increases and decreases the oscillator circuit frequency. As the vco output frequency increases, (toward 13.7997 MHz), the output frequency of the programmable divider circuit increases (toward 300 Hz) which, in turn, decreases the error voltage applied to VR4. When the oscillator output frequency reaches 13.7997 MHz, the output from the programmable divider circuit is 300 Hz (13.7997 MHz ÷ 45.999). The vco circuit locks at this frequency and remains until the bfo frequency information is changed. The 13.7997-MHz oscillator frequency is divided by 30 to produce the 459.99-kHz if output signal that is applied to if amplifier for use in the SSB, ISB, and CW modes of operation.

If the BFO is set to the maximum deviation below the operating frequency (9.990 kHz), the synthesizer functions are the same except the +/- input goes to - (logic 0) and the programmable divider circuit is set to a count-up state and begins counting at 55 000 plus the BFO offset (deviation) of 9.990 kHz or, a 55 999 start counting point. The count progresses toward a maximum count of 100 000. This produces the division ratio of 44 001 (100 000 - 55 999). The error voltage applied to VR4 decreases and causes the output frequency to decrease. When the output of the programmable divider reaches 300 Hz, the oscillator output frequency will lock at 13.2003 and, when divided by 30, will produce the 440.01-kHz vbfo output signal.

2.3 Input Control Signals

2.3.1 Parallel BCD Input (Remote control operation only.)

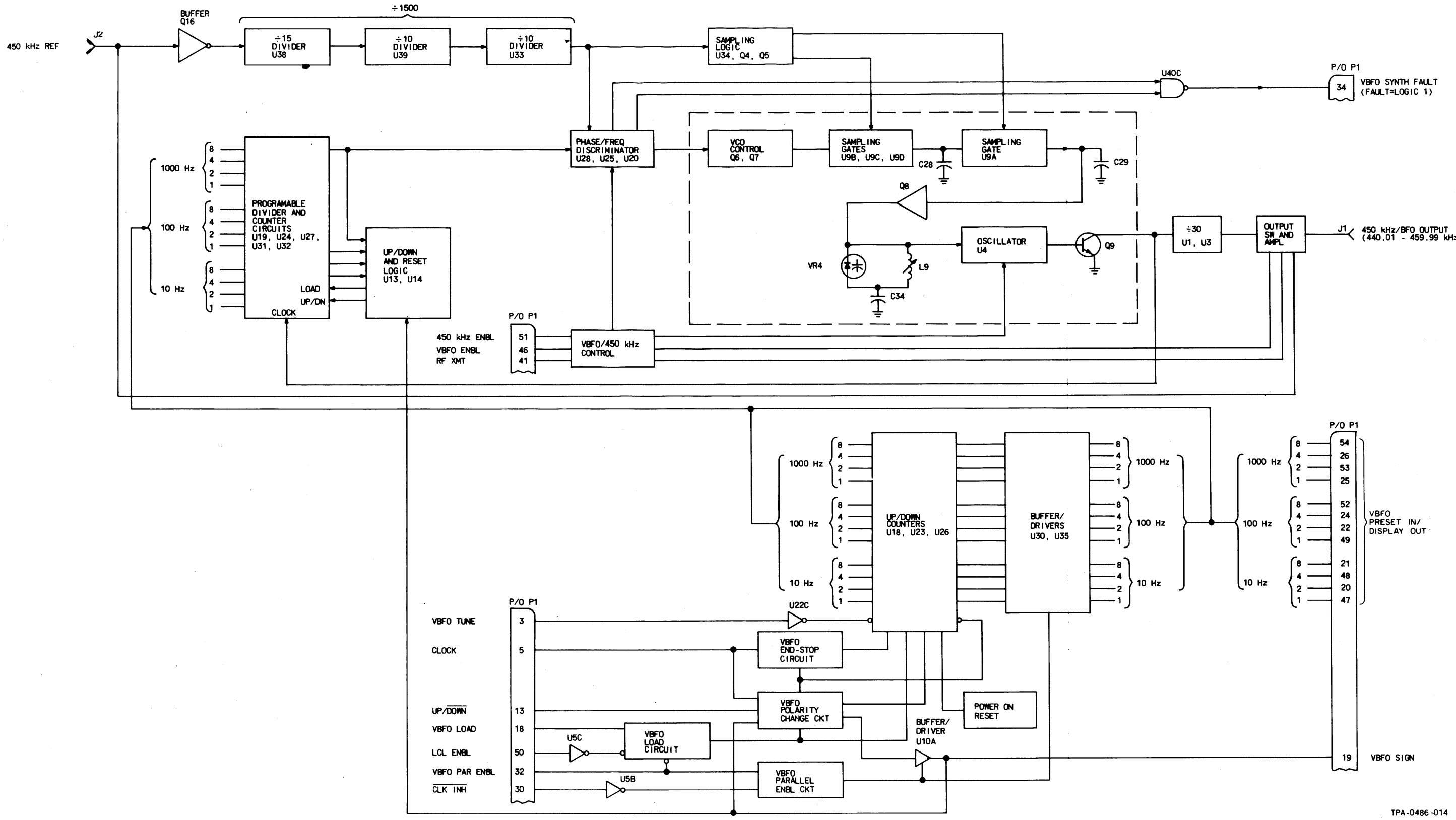
When applying the parallel bcd input signals at P1 to activate the vbfo, the vbfo parallel enable signal (logic 1) is applied at P1-32 and $\overline{\text{local enable}}$ (logic 0) is applied at P1-50. This allows the dual one-shot U6A and U6B to generate a preset enable input to the up/down counters each time a logic 1 vbfo pulse is applied to P1-18. The logic 1 preset enable input allows the up/down counters to be preset to the applied parallel input. When the preset enable is removed, the applied parallel input is stored in the up/down counters until a clock signal (C), reset signal (R), or another preset enable signal (PE) is applied.

2.3.2 VBFO Tune Input

When applying a vbfo tune input (logic 1) at P1-3 to activate the vbfo, the following signals are also applied:

a. Vbfo parallel enable (logic 0) at P1-32.
b. $\overline{\text{Clock inhibit}}$ (logic 0) at P1-30.
c. Vbfo load (logic 0) at P1-18
d. Up (logic 1) or down (logic 0) at P1-13
e. Clock at P1-5

With the above signals applied, the up/down counters count with the direction of count determined by the input at P1-13. A logic 1 input at P1-3 applies a logic 0 carry in (CI) input to counter U18, enabling the 10-Hz counter. As the clock pulses are received the counter counts.



VBFO, Block Diagram
Figure 2

When the 10-Hz count reaches 9 (on an up-count) a logic 0 carryout signal is supplied as a carry-in to the 100-Hz counter U23. On the next clock the 10-Hz counter is reset, the 100-Hz counter is clocked, and the carryout signal goes to a logic 1 stopping the count of the 100-Hz counter after 1 count. This type of sequence continues through the 10-Hz, 100-Hz, and 1000-Hz counters until a frequency bcd of 9990 (up-count) is reached. When 9990 (up-count) is reached, a carryout (logic 0) is supplied through inverter U5D to NAND gate U15C. The inverted carryout signal is NANDed with the up (logic 1) signal and supplied to U11A. In the up-count, this U11A input is logic 0 and 0Red with the inverted output of 10-Hz bcd 1 count (90 Hz = 10-Hz bcd, 8 + 1) and supplies a logic 0 to clock gate U21D. U21D is inhibited and clocking is stopped. Refer to figure 3.

When the 10-Hz count reaches 0 (on a down-count) a logic 0 carryout signal is supplied as a carry-in to the 100-Hz counter U23. On the next clock the 10-Hz counter is reset, the 100-Hz counter is clocked and the carryout signal goes to a logic 1 stopping the count of the 100-Hz counter after 1 count. This type of sequence continues through the 10-Hz, 100-Hz, and 1000-Hz counters until a frequency bcd of 0000 (down-count) is reached. When 0000 (down-count) is reached, a carryout (logic 0) is supplied through inverter U5D to up/down control circuit at U17-4, -11. A bcd $\overline{1}$ is also supplied through inverter U22B to up/down control circuit at U17-5, -10. These two inputs (k1, k2) along with the inverted down input at U17-9 (k3) allows flip-flop U17 to change states on the next clock producing a $\overline{Q}$ output which is NANDed with the k3 input causing U12B output to go to logic 0 and output of U12D to go to logic 1, initiating an up-count on the next pulse. Refer to figure 4.

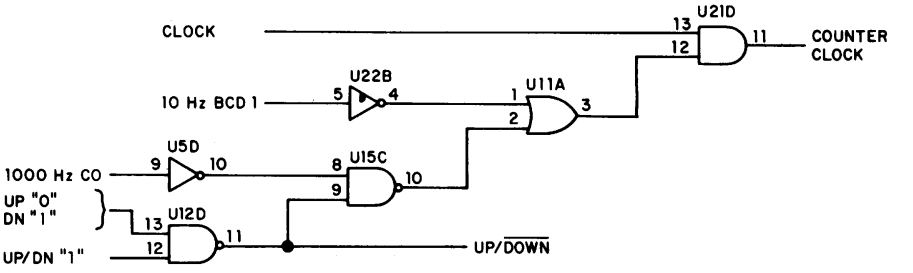
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the vbfo are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in this section check total performance of the vbfo. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



COUNT UP/DOWN	U5D		U12D			U15C			U22B		U11A			U21D			NOTES
	IN	OUT	IN		OUT	IN		OUT	IN	OUT	IN		OUT	IN		OUT	
	-9	-10	-12	-13	-11	-8	-9	-10	-5	-4	-1	-2	-3	-13	-12	-11	
9990 UP	0	1	1	0	1	1	1	0	1	0	0	0	0	CLK	0	0	INHIBITS CLK
9000 UP	1	0	1	0	1	0	1	1	1	0	0	1	1	CLK	1	CLK	CLOCK IS ENABLED
0000 UP	1	0	1	0	1	0	1	1	1	0	0	1	1	CLK	1	CLK	
0000 DN	0	1	1	1	0	0	0	1	1	0	0	0	1	CLK	1	CLK	
9000 DN	1	0	1	1	0	0	0	1	1	0	0	0	1	CLK	1	CLK	
9990 DN	1	0	1	1	0	0	0	1	0	1	1	0	1	CLK	1	CLK	

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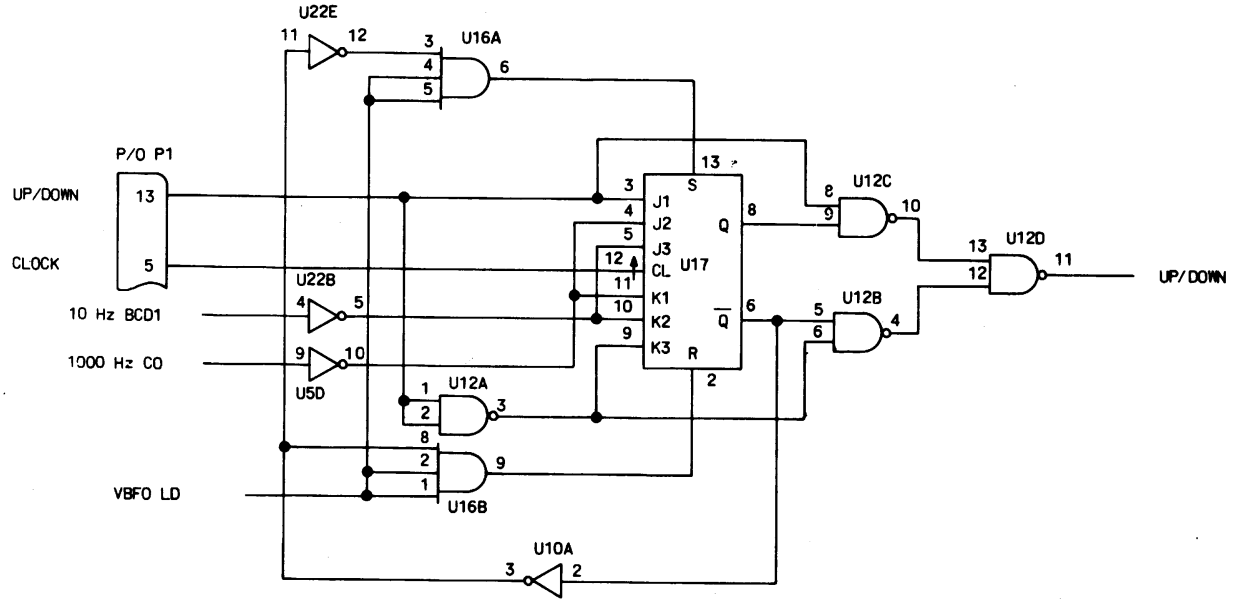
VBFO End-Stop Circuit
Figure 3



COUNT UP/DOWN	U22E		U22B		U5D		U12A		U16A			U16B			U17										U12B		U12C			U12D		
	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN		OUT	IN		OUT	S	R	J1	J2	J3	K1	K2	K3	Q	$\overline{Q}$	IN	OUT	IN	OUT	IN		OUT
	-11	-12	4	5	9	10	1	3	3	4	6	1	8	9	13	2	3	4	5	11	10	9	8	6	5	6	4	8	9	10	-12	-13	-11
9990 UP	1	0	1	0	1	0	1	0	0	1	1	1	1	0	1	0	1	0	0	1	0	0	0	1	1	0	1	1	0	1	1	0	1
9000 UP	1	0	0	1	0	1	1	0	0	1	1	1	1	0	1	0	1	1	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1
0000 UP	1	0	0	1	0	1	1	0	0	1	1	1	1	0	1	0	1	1	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1
0000 DN	0	1	0	1	1	0	0	1	1	1	0	1	0	1	0	1	0	0	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0
9000 DN	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1	1	0	0	1	1	0	1	1	1	1	0
9990 DN	0	1	1	0	0	1	0	1	1	1	0	1	0	1	0	1	0	1	0	0	0	1	1	0	0	1	1	0	1	1	1	1	0

NOTE:

WHEN 0000 DOWN COUNT IS REACHED, THE ABOVE LOGIC CIRCUITS ARE SET UP TO CHANGE DIRECTION (DOWN TO UP). WITH THE NEXT CLOCK INPUT (AFTER DOWN 0000) U17 CHANGES OUTPUT STATES. WHEN $\overline{Q}$ GOES TO LOGIC 1 U22E AND U16B SET U17 AND HOLD IT IN THE UP COUNT STATE.

TPA-0485-014

VBFO Polarity Change Circuit
Figure 4

Table 1. VBFO, Testing, and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the vbfo that is to be tested. b. If installed, remove parallel input, parallel output, and serial interface. **Note** If removed, upon completion of control testing, reinstall parallel input, parallel output, and serial interface. c. Remove vbfo card. Install it on an extender card and place it in the unit. d. Set unit LINE SELECTOR for power source available (100/115/215/230 V ac). **Note** Ensure that proper fuse is installed for power source used. e. Connect unit to available power source.		
2. Initial check	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to HOLD. AGC to FAST. RF GAIN to full cw. b. Measure dc voltages between the following points and ground (TP1). P1-23 P1-27 c. Measure dc voltage between points A and B (as shown in figure 5). **Note** If external keep-alive voltage is connected to unit under test, perform step 2.d. d. Measure dc voltage between P1-45 and ground (TP1).	 +15 ±1.0 V dc. +5 ±0.5 V dc. NMT 0.2 V dc. **Note** Point A is 5-V dc keep-alive voltage. Point B is 5-V dc supply voltage. +5.0 to +12.0 V dc (depending on source used).	 Check associated power supply. Check Q3 and associated circuit. Check associated power supply.

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. VBFO/450-kHz output switch

(Cont)</td><td>a. Front-panel controls set as follows:

PWR to on.
CONT to LCL.
MODE to AM.
BANDWIDTH to 16.
DIAL to FINE.
BFO to FIX.
AGC to OFF.
RF GAIN to full cw.

Note

Logic 1 = NLT +3.0 V dc.

Logic 0 = NMT 0.5 V dc.

b. Note logic level at TP8.

c. Note output frequency at J1.

d. Repeat steps 3.b and 3.c at each of the following conditions:

<table><tr><th>MODE SWITCH</th><th>BFO SWITCH</th><th>TP8</th><th>J1</th></tr><tr><td>AM
SSB/CW
SSB/CW</td><td>TUNE
FIX
TUNE</td><td>Logic 0
Logic 0
Logic 1</td><td>0 Hz
450 kHz
*Vbfo</td></tr><tr><td colspan="4">*Vbfo frequency equals 450 kHz plus the algebraic sum of the vbfo offset.</td></tr></table>
Caution

In the following procedures, when applying +5 V dc or 0 V dc (ground) to the indicated points, apply these levels through a 100-ohm series limiting resistor. The +5-V dc source should be obtained from the receiver power supply so that the integrated circuit supply voltages are not exceeded by the applied levels.

Note

450-kHz enable (P1-51).

e. Apply +5 V dc to TP4 (rf xmt).</td><td>Logic 0

0 Hz</td><td>Check U21 and associated circuit.

Check U21, U29, and associated circuits.

Same as step 3.b and 3.c.</td></tr>
</table>

Table 1. VBFO, Testing, and Troubleshooting Procedures. (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	f. Repeat steps 3.b and 3.c at each of the following conditions:		Same as step 3.b and 3.c.

MODE SWITCH	BFO SWITCH	TP8	J1
AM	FIX	Logic 0	0 Hz
AM	TUNE	Logic 0	0 Hz
SSB/CW	FIX	Logic 0	450 kHz
SSB/CW	TUNE	Logic 1	450 kHz

g. Remove +5 V dc from TP4.		
h. Connect a spectrum analyzer to J1.		
i. Set VBFO OFFSET HZ from 1000 Hz.		
j. Note level of 451-kHz if signal at J1.	Reference.	
k. Measure level of sidebands caused by 300-Hz VBFO reference signal at J1.	NLT 70 dB below 451-kHz reference.	Check bypass and feedthrough capacitors and circuits associated with J1 output or return to factory for repair.
l. Apply +5 V dc to TP4 (rf xmt).		
m. Measure level of 451 kHz if signal at J1.	NLT 70 dB below reference in step 3.j.	Check U29A and associated circuits.
n. Note level of 450 kHz if signal at J1.	Reference.	
o. Remove +5 V dc from TP4.		
p. Measure level of 450-kHz if signal at J1.	NLT 70 dB below reference in step 3.n.	Check U29D and associated circuits.
q. Set VBFO OFFSET HZ for 9990 Hz.		
r. Using a distortion analyzer, measure total harmonic distortion at J1.		
s. Set VBFO OFFSET HZ for 0000 Hz.		
t. Measure total harmonic distortion at J1.	NMT 3%.	Same as step 3.k.
u. Apply +5 V dc to TP4 (rf xmt).		
v. Measure total harmonic distortion at J1.	NMT 3%.	Same as step 3.k.
w. Remove +5 V dc from TP4.		

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Frequency accuracy	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Connect a frequency counter to J1.		
	c. Measure the frequency outputs listed below. Check both positive and negative offset.	±5 Hz of listed output.	Check phase-lock loop.
	d. At each frequency measure vbfo synthesizer fault output using a dvm connected at TP2.	NMT 0.5 V dc.	Check U40C and associated circuit.

OFFSET (Hz)	OUTPUT FREQUENCY	
	POSITIVE OFFSET	NEGATIVE OFFSET
9990	459.99 kHz	440.01 kHz
9980	459.98 kHz	440.02 kHz
9970	459.97 kHz	440.03 kHz
9960	459.96 kHz	440.04 kHz
9950	459.95 kHz	440.05 kHz
9940	459.94 kHz	440.06 kHz
9930	459.93 kHz	440.07 kHz
9920	459.92 kHz	440.08 kHz
9910	459.91 kHz	440.09 kHz
9900	459.90 kHz	440.10 kHz
9800	459.80 kHz	440.20 kHz
9700	459.70 kHz	440.30 kHz
9600	459.60 kHz	440.40 kHz
9500	459.50 kHz	440.50 kHz
9400	459.40 kHz	440.60 kHz
9300	459.30 kHz	440.70 kHz
9200	459.20 kHz	440.80 kHz
9100	459.10 kHz	440.90 kHz
9000	459.00 kHz	441.00 kHz
8000	458.00 kHz	442.00 kHz
7000	457.00 kHz	443.00 kHz
6000	456.00 kHz	444.00 kHz
5000	455.00 kHz	445.00 kHz
4000	454.00 kHz	446.00 kHz
3000	453.00 kHz	447.00 kHz
2000	452.00 kHz	448.00 kHz
1000	451.00 kHz	449.00 kHz
0000	450.00 kHz	450.00 kHz

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Local operation	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Connect an oscilloscope to TP5.		
	c. Note display on oscilloscope while rotating front-panel TUNING knob.	Clock pulses are continuous when TUNING knob is rotated between --9990 and +9990 VBFO OFFSET HZ. When VBFO OFFSET HZ reaches -9990 or +9990, clock pulses cease until the TUNING knob is rotated in the opposite direction. Frequency of clock pulses is increased by rotating the TUNING knob faster and decreased by rotating the TUNING knob slower.	Check U17, U21D, and associated circuit.
	d. Note display on oscilloscope while rotating front-panel TUNING knob. Set BFO switch to HOLD.	Clock pulses cease when BFO switch is set to HOLD. VBFO OFFSET HZ does not change while BFO is in HOLD position.	Check U18, U23, U26, U5D, U22C, and associated circuit.
	e. Set BFO switch to TUNE.		
	f. Apply +5 V dc to P1-32 (vbfo parallel enable).	VBFO OFFSET HZ display blanks.	Check U30, U35, and associated circuit.
	g. Remove +5 V dc from P1-32.	VBFO OFFSET HZ display lights on same frequency as before blanking.	Check U6, U18, U23, U26, U5C, and associated circuit.
(Cont)	h. Connect a ground to P1-30 ($\overline{\text{clock inhibit}}$).	VBFO OFFSET HZ display blanks.	Same as step 5.f.

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	i. Remove P1-30 ground.	VBFO OFFSET HZ display lights on same frequency as before blanking.	Same as step 5.g.
	j. Note display on oscilloscope while rotating front-panel TUNING knob. Set CONT switch to REM.	CONT switch positioning has no effect on clock pulses.	Check U21D, U11A, and associated circuit.
6. Remote control	a. Front-panel controls set as follows: PWR to ON. CONT to REM. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Apply +5 V dc to P1-32 (vbfo parallel enable).		
	c. Connect an oscilloscope to TP7.		
	d. Momentarily apply +5 V dc to P1-18 (vbfo load).	Pulse at TP7 should be NLT 5 μs and NMT 20 μs.	Check U5C, U6, and associated circuit.
	e. Set CONT switch to LCL.		
	f. Repeat step d.	No pulse at TP7.	Same as step 6.d.
	g. Set CONT switch to REM.		
	h. Remove +5 V dc from P1-32.		
	i. Repeat step d.	No pulse at TP7.	Same as step 6.d.
(Cont)	j. Refer to chart and apply bcd frequency for -1230 vbfo offset frequency.		

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

6. (Cont)

VBFO OFFSET HZ	VBFO BCD FREQUENCY (HZ)												VBFO SIGN
	1000				100				10				
	8	4	2	1	8	4	2	1	8	4	2	1	
	P1-( )												
	54	26	53	25	52	24	22	49	21	48	20	47	19
-1230	0	0	0	1	0	0	1	0	0	0	1	1	0
0000	0	0	0	0	0	0	0	0	0	0	0	0	1 or 0
+9990	1	0	0	1	1	0	0	1	1	0	0	1	0
-9990	1	0	0	1	1	0	0	1	1	0	0	1	1
+8760	0	1	0	0	0	1	1	1	0	1	1	0	0
-2340	0	0	1	0	0	0	1	1	0	1	0	0	1

Logic 1 = NLT + 3.0 V dc; Logic 0 = NMT 0.5 V dc.

k. Apply +5 V dc to P1-32 (vbfo parallel enable).		
l. Momentarily apply +5 V dc to P1-18 (vbfo load).	VBFO OFFSET HZ display indicates -1230.	Check inputs.
m. Remove -1230 bcd frequency input. (with no logic 1's applied, vbfo bcd frequency is pulled-down to all logic 0's.	VBFO OFFSET HZ display indicates 0000.	Check associated pull-down circuit.
n. Remove +5 V dc from P1-32.		
o. Set CONT switch to LCL.	VBFO OFFSET HZ display indicates -1230.	Check U18, U23, U26, and associated circuit.
p. Rotate TUNING knob each direction from set frequency.	Counter clockwise counts down, clockwise counts up.	Check input to P1-13 (Logic 1 = up; logic 0 = down), if okay check U17 and associated circuit.
(Cont) q. Set CONT switch to REM.		

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont)

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)	r. Repeat steps 6.j thru 6.q. at each bcd frequency listed in chart.	VBFO OFFSET HZ display indicates vbfo bcd frequency applied in step 6.j. for steps 6.l and 6.o. VBFO OFFSET HZ display indicates 0000 for step 6.m. Step 6.p at -9990 will not count down and at +9999 will not count up.	Same as steps 6.j. thru 6.q.
7. Vbfo synthesizer fault	a. Front-panel controls set as follows: PWR to ON. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Using TUNING knob set VBFO OFFSET HZ to 00.		
	c. Measure output at P1-34 (vbfo synthesizer fault).	NMT 0.5 V dc.	Check U20 and associated circuit.
	d. Disconnect 450-kHz reference at J2.		
	e. Measure output at P1-34.	NLT +3.0 V dc.	Same as step 7.c.
	f. Reconnect 450-kHz reference at J2.		
	g. Measure output at P1-34.	NMT 0.5 V dc.	Same as step 7.c.
	h. Repeat steps 7.c thru 7.g with VBFO OFFSET HZ at each of the following settings: +7770 +3330 -3330 -7770	Same as steps 7.c thru 7.g.	Same as step 7.c.
8. External keep-alive (Cont)	a. Front-panel controls set as follows: PWR to ON. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. (Cont)	b. Apply external keep-alive voltage (6 to 12 V dc) to rear panel of unit at TB3-4 (+) and TB3-5 (-). c. Set PWR to off. d. Measure dc voltage at capacitor C9 positive (+) lead. e. Remove external keep-alive voltage.	 7.0 ±1.5 V dc.	 Check CR3, CR2, Q1, and associated circuit.
9. Internal keep-alive	a. Front-panel controls set as follows: PWR to ON. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw. b. Using TUNING knob set VBFO OFFSET HZ to +7770. c. Set BFO to HOLD. d. Set PWR to off. e. After 5 minutes with PWR off, set PWR to on.	 VBFO OFFSET HZ display indicates +7770.	 Check C9 and associated circuits.
10. Test complete	a. Set PWR switch off. b. Disconnect external power from rear panel. c. Remove vbfo from extender and extender from unit. d. Reinstall vbfo in unit. e. If removed in setup, reinstall parallel input, parallel output, and serial interface. f. Reinstall unit top cover.		

4. ALIGNMENT/ADJUSTMENT.

4.1 Voltage Adjustment

a. Perform table 1, test 1 and test 2.
b. Connect a dvm between bottom end of R28 and ground (TP1).
c. Set front-panel controls as follows:

PWR to on.
CONT to LCL.
MODE to SSB/CW.
BANDWIDTH to 16.
DIAL to FINE.
BFO to TUNE.
AGC to OFF.
RF GAIN to full cw.

d. Adjust R7 for 12.0 ±0.1 V dc at R28.
e. Remove dvm.

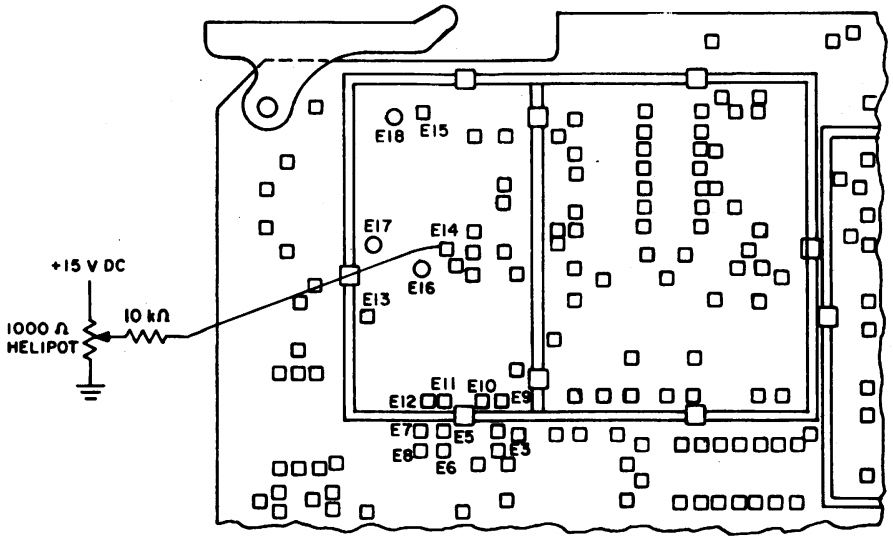
4.1 Oscillator Adjustments.

Note

To perform these adjustments, the oscillator can shield must be removed. Do not make these adjustments unless a repair has been made and necessary adjustment is indicated.

4.2.1 Oscillator Adjustment.

a. Perform table 1, test 2 and test 2.
b. Adjust R30 and R37 to maximum cw position.
c. Connect a helipot to C29, as shown in figure 5.



TPA-1361-011

Setup for Oscillator Adjustments
Figure 5

d. Connect a dvm to C29 (where helipot is connected.).
e. Apply a ground at bottom end of R13.
f. Connect a frequency counter at J1.
g. Set front-panel controls as follows:

PWR to on.
CONT to LCL.
MODE to SSB/CW.
BANDWIDTH to 16.
DIAL to FINE.
BFO to TUNE.
AGC to OFF.
RF GAIN to full cw.

i. Adjust the helipot for 5.5 ±0.1 V dc at C29.
j. Adjust L9 for a frequency of 450.0 ±0.33 kHz at J1. Tuning slug should be toward the top of L9.

4.2.2 Frequency Range

a. Adjust the helipot for 3.5 ±0.1 V dc at C29. Frequency should be 460.00 kHz minimum.
b. Adjust the helipot for 7.3 ±0.1 V dc at C29. Frequency should be 440.00 kHz maximum.

Note

If step a or b is out of range, readjustment of L9 in the direction of the range error could correct the problem. If both steps a and b are out of range, repair is indicated.

c. Remove helipot, dvm, and frequency counter.
d. Remove R13 ground.

4.3 Output Level

a. Perform table 1, test 1 and test 2.
b. Connect an rf voltmeter (with 50-Ω load) to J1.
c. Set front-panel controls as follows:
PWR to on.
CONT to LCL
MODE to SSB/CW.
BANDWIDTH to 16.
DIAL to FINE.
BFO to TUNE.
AGC to OFF.
RF GAIN to full cw.
d. Adjust R30 for 300 ±10 mV rms at J1.
e. Apply +5 V dc at TP4 (yellow).
f. Adjust R37 for 300 ±10 mV rms at J1.
g. Remove +5 V dc from TP4.
h. Remove rf voltmeter.

5. REPAIR

Repair of the vbfo is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

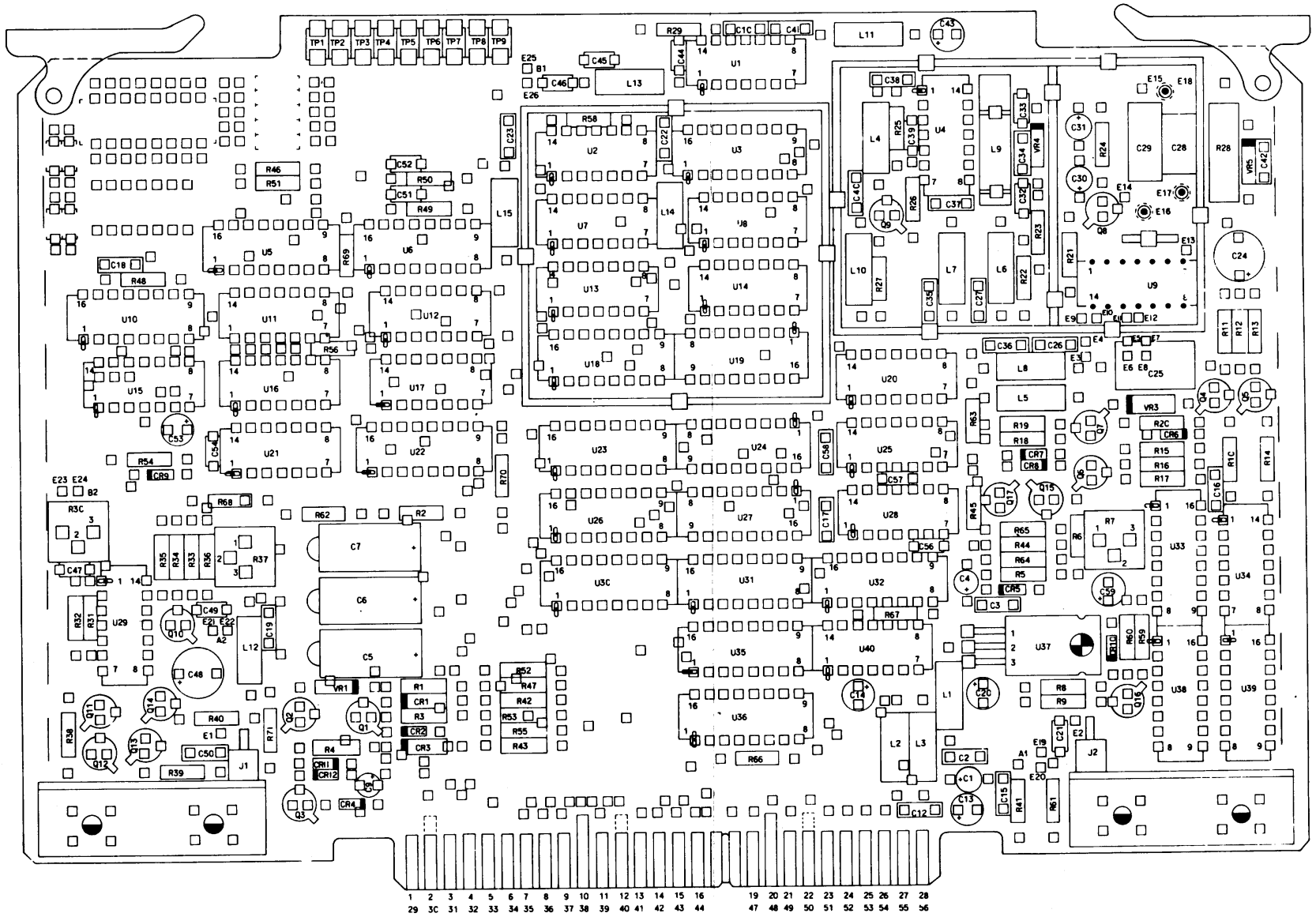
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 6). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Vbfo	638-6067-001	REV D



TPA-0809-019

VBFO, Schematic Diagram
Figure 6 (Sheet 1 of 4

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	VBFO A4	638-6067-001	
CR1	SEMICOND DEVICE 1N3070	353-3083-000	
CR2	SEMICOND DEVICE 1N3070 (A3)	353-3083-000	
CR2	SEMICOND DEVICE 1N4454	353-3644-010	
CR3	SEMICOND DEVICE 1N3070	353-3083-000	
CR4-CR10	SEMICOND DEVICE 1N4454	353-3644-010	
CR11, CR12	SEMICOND DEVICE 1N4454 (A3)	353-3644-010	
C1	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C2,C3	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C4	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C5-C7	CAPACITOR,FXD ELCTLT, 330UF, PORM20%, 20V	184-9117-040	
C8	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V (A3)	913-5019-440	
C9	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C10	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C11	NOT USED		
C12	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C13	CAPACITOR,FXD ELCTLT, 4.7UF, 20%, 35V	184-9102-390	
C14	CAPACITOR,FXD ELCTLT, 22UF, 20%, 10V	184-9102-080	
C15-C19	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C20	CAPACITOR,FXD ELCTLT, 15UF, 20%, 20V	184-9102-180	
C21	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C22,C23	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C24	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-190	
C25	CAPACITOR,FXD PLSTC DIEL, 0.47UF, 5%, 50V	933-1084-210	
C26,C27	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C28	CAPACITOR,FXD PLSTC DIEL, 0.1UF, 10%, 50V	933-1081-080	
C29	CAPACITOR,FXD PLSTC DIEL, 0.047UF, 10%, 50V	933-1043-500	
C30,C31	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C32,C33	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C34-C38	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C39	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C40-C42	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C43	CAPACITOR,FXD ELCTLT, 22UF, 20%, 10V	184-9102-080	
C44	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C45,C46	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C47	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C48	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-190	
C49	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C50	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C51,C52	CAPACITOR,FXD CER DIEL, 100PF, 10%, 200V	913-4006-000	
C53	CAPACITOR,FXD ELCTLT, 10UF, 20%, 25V	184-9102-240	
C54	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C55	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V (A2)	913-4018-000	
C56,C57	CAPACITOR,FXD CER DIEL, 100PF, 10%, 200V	913-4006-000	
C58	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C59	CAPACITOR,FXD ELCTLT, 10UF, 20%, 25V (A4)	184-9102-240	
C60	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V (A5)	913-5019-440	
J1,J2	CONNECTOR,RCPT ELEC	357-7207-100	
L1	COIL,RF 33UH	240-2715-310	
L2,L3	COIL,RF 1UH	240-2715-130	
L4-L8	COIL,RF 10UH	240-2715-250	
L9	COIL,RF,VAR 2.4 TO 3.6UH	240-2739-010	
L10,L11	COIL,RF 10UH	240-2715-250	
L12	COIL,RF 1000UH	240-2715-490	
L13	COIL,RF 330UH	240-2715-430	
L14,L15	COIL,RF 10UH	240-2715-250	
Q1	TRANSISTOR 2N4091	352-0759-010	
Q2-Q5	TRANSISTOR 2N2222A	352-0661-020	
Q6	TRANSISTOR 2N2907A	352-0551-010	
Q7	TRANSISTOR 2N2222A	352-0661-020	
Q8	SEMICOND DEVICE 2N3796	352-1018-010	
Q9	TRANSISTOR 2N2369A	352-0596-030	
Q10-Q17	TRANSISTOR 2N2222A	352-0661-020	
R1	RESISTOR,FXD CMPSN, 33 OHMS, 10%, 1/4W	745-0695-000	
R2	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W (A3)	745-0821-000	
R2	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R3	RESISTOR,FXD CMPSN, 0.15MEGO, 10%, 1/4W (A3)	745-0827-000	
R3	RESISTOR,FXD CMPSN, 33K, 10%, 1/4W	745-0803-000	
R4	RESISTOR,FXD CMPSN, 22K, 10%, 1/4W (A3)	745-0797-000	
R4	RESISTOR,FXD CMPSN, 27K, 10%, 1/4W	745-0800-000	
R5	RESISTOR,FXD FILM, 243 OHMS, 1%, 1/8W (A4)	705-3600-670	
R5	RESISTOR,FXD FILM, 226 OHMS, 1%, 1/8W	705-0965-000	
R6	RESISTOR,FXD FILM, 1.91K, 1%, 1/8W	705-3605-130	
R7	RESISTOR,VAR 200 OHMS, 20%, 1/2W	382-0038-020	
R8	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R9	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R10	RESISTOR,FXD CMPSN, 5.6K, 10%, 1/4W	745-0776-000	
R11	RESISTOR,FXD CMPSN, 15K, 10%, 1/4W	745-0791-000	
R12	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R13	RESISTOR,FXD CMPSN, 15K, 10%, 1/4W	745-0791-000	
R14	RESISTOR,FXD CMPSN, 5.6K, 10%, 1/4W	745-0776-000	
R15	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/4W	745-0731-000	
R16	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R17	RESISTOR,FXD CMPSN, 68 OHMS, 10%, 1/4W	745-0707-000	
R18	RESISTOR,FXD CMPSN, 5.6K, 10%, 1/4W	745-0776-000	
R19	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/4W	745-0755-000	
R20	RESISTOR,FXD CMPSN, 33 OHMS, 10%, 1/4W	745-0695-000	
R21	RESISTOR,FXD FILM, 14.7K, 1%, 1/8W	705-1052-000	
R22	RESISTOR,FXD FILM, 31.6K, 1%, 1/8W	705-1068-000	
R23	RESISTOR,FXD FILM, 46.4K, 1%, 1/8W	705-1076-000	
R24	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R25	RESISTOR,FXD CMPSN, 3.9K, 10%, 1/4W	745-0770-000	
R26	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R27	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W (A4)	745-0713-000	

PARTS LIST (Cont)

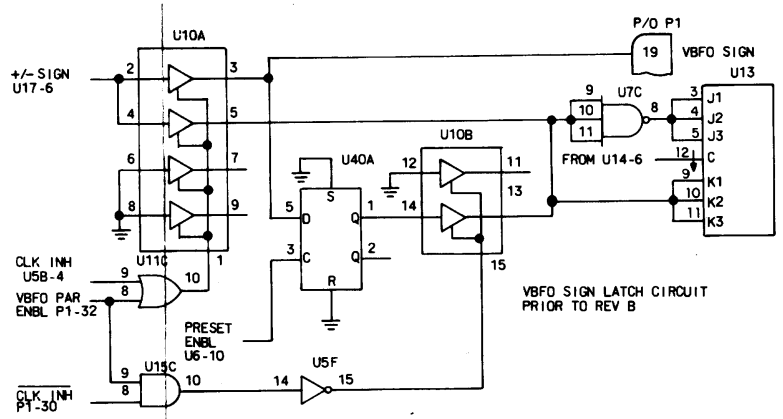
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R27	RESISTOR,FXD CMPSN, 180 OHMS, 10%, 1/4W	745-0722-000	
R28	RESISTOR,FXD FILM, 20.5K, 1%, 1/8W	705-1059-000	
R29	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/4W (A4)	745-0761-000	
R29	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/4W	745-0755-000	
R30	RESISTOR,VAR 1K, 20%, 1/2W	382-0038-040	
R31	RESISTOR,FXD CMPSN, 27K, 10%, 1/4W	745-0800-000	
R32	RESISTOR,FXD CMPSN, 33K, 10%, 1/4W (A4)	745-0803-000	
R32	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R33	RESISTOR,FXD CMPSN, 15K, 10%, 1/4W	745-0791-000	
R34	RESISTOR,FXD CMPSN, 12K, 10%, 1/4W	745-0788-000	
R35	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R36	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/4W (A4)	745-0746-000	
R36	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/4W	745-0743-000	
R37	RESISTOR,VAR 200 OHMS, 20%, 1/2W (A4)	382-0038-020	
R37	RESISTOR,VAR 1K, 20%, 1/2W	382-0038-040	
R38	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R39	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R40	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R41	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W (A4)	745-0785-000	
R41	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R42,R43	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R44	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W (A4)	745-0857-000	
R44	RESISTOR,FXD CMPSN, 56K, 10%, 1/4W	745-0812-000	
R45	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R46-R48	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R49,R50	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/4W (A4)	745-0773-000	
R49,R50	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R51-R53	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R54	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R55	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R56	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R57	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W (A6)	745-0821-000	
R58-R60	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R61	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R62	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W (A3)	745-0749-000	
R62	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R63,R64	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R65	RESISTOR,FXD CMPSN, 56K, 10%, 1/4W	745-0812-000	
R66	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W (A4)	745-0857-000	
R67	RESISTOR,FXD CMPSN, 56K, 10%, 1/4W (A4)	745-0812-000	
R68-R70	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W (A4)	745-0857-000	
TP1	JACK,TIP BRN	360-0484-070	
TP2	JACK,TIP RED	360-0484-020	
TP3	JACK,TIP ORN	360-0484-050	
TP4	JACK,TIP YEL	360-0484-060	
TP5	JACK,TIP GRN	360-0484-040	
TP6	JACK,TIP BLU	360-0484-080	
TP7	JACK,TIP VIO	360-0484-090	
TP8	JACK,TIP GRA	360-0484-100	
TP9	JACK,TIP WHT	360-0484-010	
U1	INTEGRATED CKT SN74LS90N	351-1636-010	
U2	INTEGRATED CKT SN74LS21N	351-1785-010	
U3	INTEGRATED CKT 74H106PC	351-7766-010	
U4	INTEGRATED CKT MC1648010	351-7768-010	
U5	INTEGRATED CKT F4049BPC	351-8159-210	
U6	INTEGRATED CKT MC14528BCP	351-8421-020	
U7	INTEGRATED CKT DM74LS10N	351-1523-230	
U8	INTEGRATED CKT N74LS00N	351-1523-110	
U9	INTEGRATED CKT MC14066BCP	351-8252-010	
U10	INTEGRATED CKT MC14503BCP	351-8490-010	
U11	INTEGRATED CKT MC14071BCP	351-8287-010	
U12	INTEGRATED CKT MC14011CP	351-8159-040	
U13,U14	INTEGRATED CKT 74H102	351-7767-010	
U15	INTEGRATED CKT CD4081BE (A1)	351-8287-030	
U15	INTEGRATED CKT MC14011CP	351-8159-040	
U16	INTEGRATED CKT MC14073BCP	351-8287-060	
U17	INTEGRATED CKT CD4095BE	351-8537-010	
U18	INTEGRATED CKT CD14510BCN	351-8497-010	
U19	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U19	INTEGRATED CKT SN74LS190N	351-1948-010	
U20	INTEGRATED CKT N74LS74N883C	351-1525-040	
U21	INTEGRATED CKT MC14081BCP	351-8287-030	
U22	INTEGRATED CKT F4049BPC	351-8159-210	
U23	INTEGRATED CKT CD14510BCN	351-8497-010	
U24	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U24	INTEGRATED CKT SN74LS190N	351-1948-010	
U25	INTEGRATED CKT N74LS00N	351-1523-010	
U26	INTEGRATED CKT CD4510BCN	351-8497-010	
U27	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U27	INTEGRATED CKT SN74LS190N	351-1948-010	
U28	INTEGRATED CKT N74LS74N883C	351-1525-040	
U29	INTEGRATED CKT MC14066BCP	351-8252-010	
U30	INTEGRATED CKT MC14503BCP	351-8490-010	
U31-U33	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U31-U33	INTEGRATED CKT SN74LS190N	351-1948-010	
U34	INTEGRATED CKT DM74LS10N	351-1523-230	
U35	INTEGRATED CKT MC14503BCP	351-8490-010	
U36	RESISTOR NTWK 220K, 5%, 1.25W PKG	350-4030-010	
U37	INTEGRATED,CKT LM317T	351-1271-010	
U38	INTEGRATED CKT SN74LS193N	351-1527-060	
U39	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U39	INTEGRATED CKT SN74LS190N	351-1948-010	
U40	INTEGRATED CKT F4013BPC (A1)	351-8159-110	
U40	INTEGRATED CKT MC14011UBPC (A4)	351-8159-040	
U41	INTEGRATED CKT MC14011UBPC (A4)	351-8159-040	

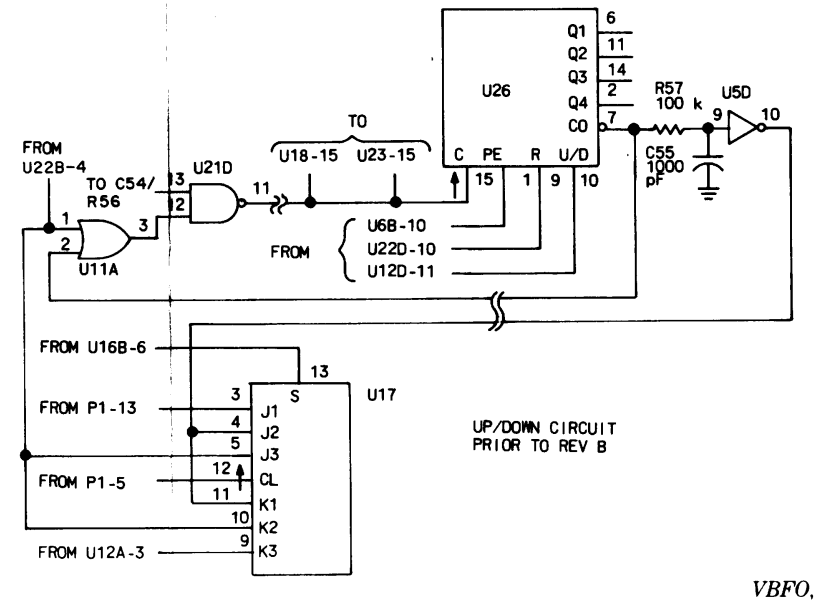
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
VR1	SEMICOND DEVICE 1N4625 (A3)	353-3591-490	
VR1	SEMICOND DEVICE 1N4104	353-3591-060	
VR2	SEMICOND DEVICE 1N4627 (A3)	353-3591-510	
VR3	SEMICOND DEVICE 1N758A	353-2724-000	
VR4	SEMICOND DEVICE 1N5148A	922-6095-200	
VR5	SEMICOND DEVICE 1N4625	353-3591-490	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
	Note Changes A1 thru A4 may have been factory installed in some units prior to REV B. Inspection of the unit will determine if these changes are installed.	
A1	VBFO sign latch circuit changed. Circuit was as shown in diagram below. Deleted U40, type F4013BPC. Changed U15 from type CD4081BE to type MC14011CP.	REV B and above
A2	Up/down circuit changed. Circuit was a shown in diagram below. Deleted C55,00pF	REV B and above

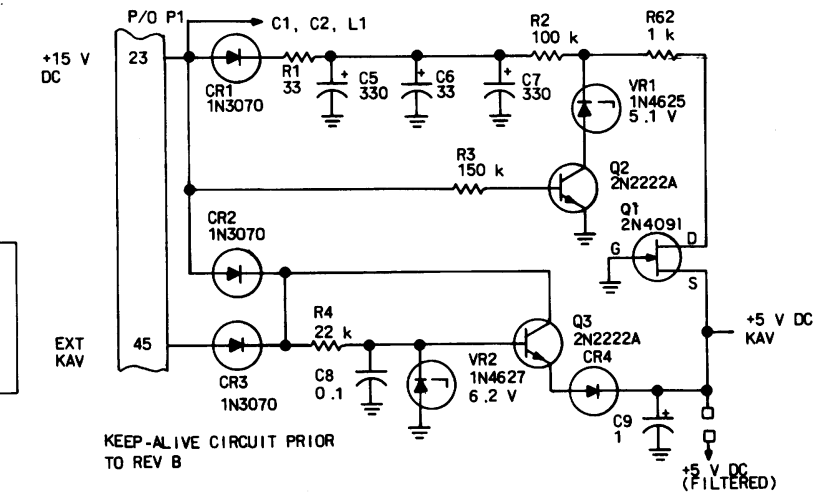




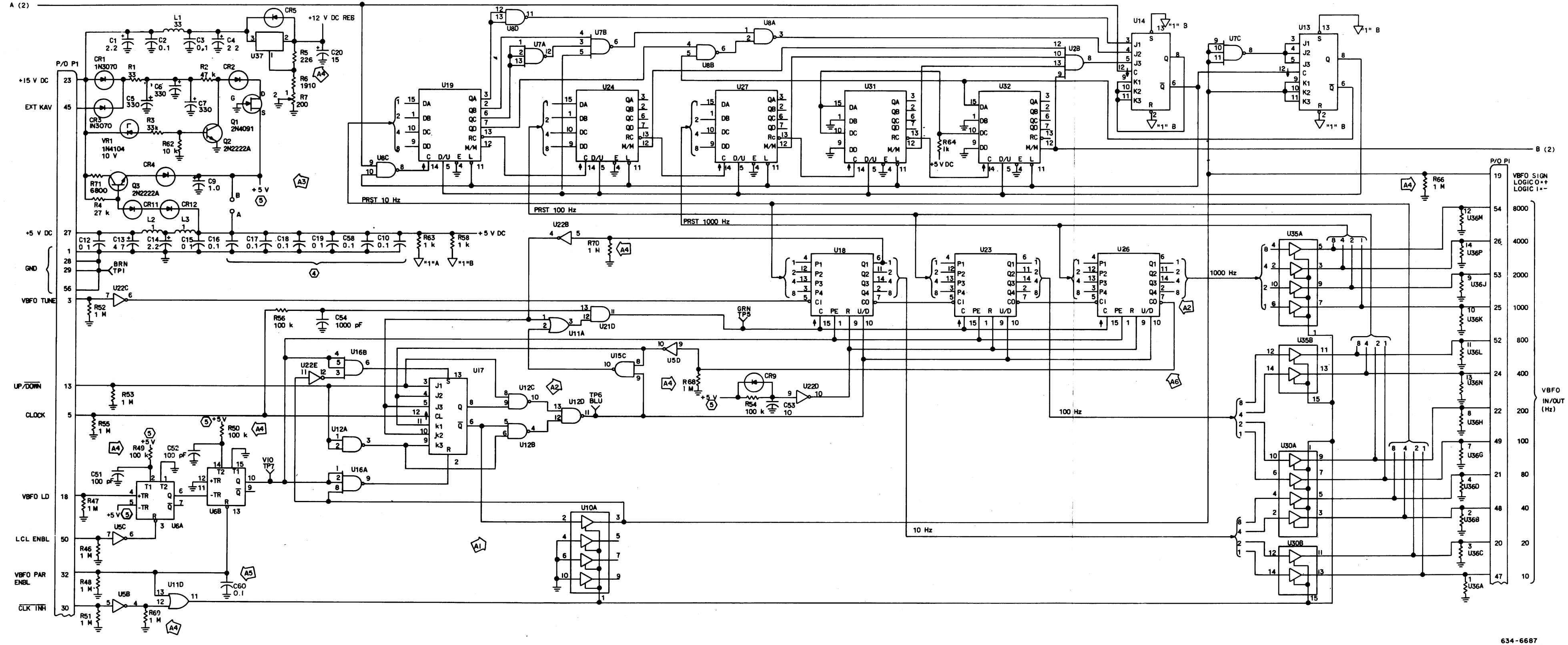
VBFO, Schematic Diagram
Figure 6 (Sheet 2)

MODIFICATION HISTORY (Cont)

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A3	External KAV (keep-alive voltage) circuit changed. Circuit was as shown in diagram below. Deleted: C8, 0.1μF. VR2, type IN4627. Changed: CR2 from type IN3070 to type IN4454. R2 from 100kΩ to 47kΩ. R3 from 150kΩ to 33kΩ. R4 from 22kΩ to 27kΩ. R62 from 1kΩ to 10kΩ. VR1 from type IN4625 to type IN4104 Added: CR11, type IN4454. CR12, type IN4454. R71, 6800Ω.	REV B and above

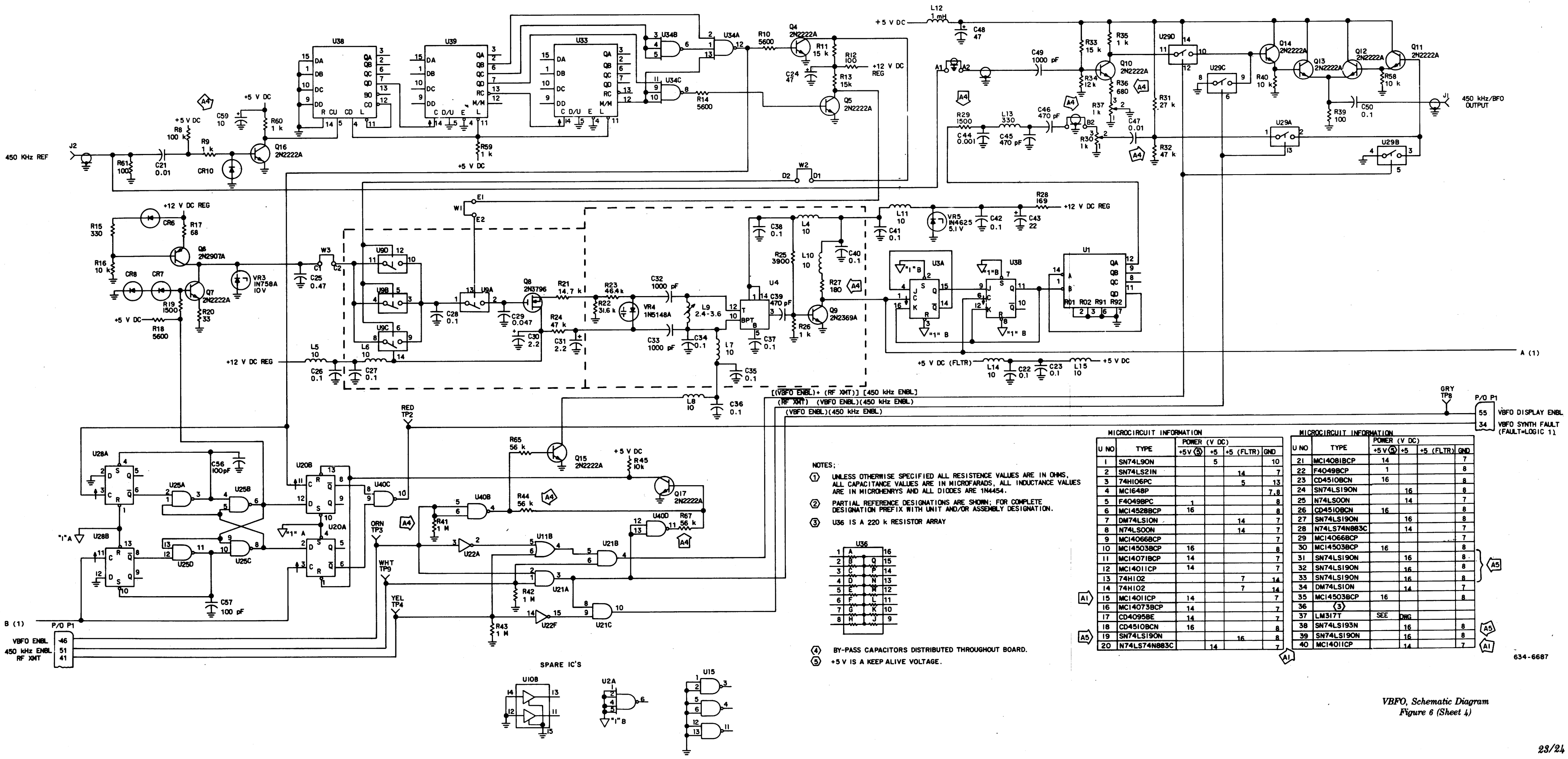


A4	Changed: R5 from 243Ω to 226Ω. R27 from 100Ω to 180Ω. R29 from 2200Ω to 1500Ω. R32 from 33kΩ to 47kΩ. R36 from 820Ω to 680Ω. R37 from 200Ω variable to 1kΩ variable. R41 from 10kΩ to 1MΩ. R44 from 1MΩ to 56kΩ. R49 from 4700Ω to 100kΩ. R50 from 4700Ω to 100kΩ. U41, type MC14011CP to U40, type MC14011CP Added: C59, 10μF. R66, 1MΩ. R67, 56kΩ. R68, 1MΩ. R69, 1MΩ. R70, 1MΩ.	REV B and above.
A5	Changed U19, U24, U27, U31, U32, U33, and U39 from type SN74LS190N to type Added C60, 0.1μF.	REV C and above.
A6	Deleted R57, 100kΩ from in series with U26-7 and U5D-9.	REV D and above.



634-6687

VBFO, Schematic Diagram
Figure 6 (Sheet 3)



MICROCIRCUIT INFORMATION

U NO	TYPE	POWER (V DC) +5V (5)	+5	+5 (FLTR)	GND
1	SN74L90N		5		10
2	SN74LS21N			14	7
3	74H106PC			5	13
4	MC1648P				7,8
5	F4049BPC	1			8
6	MC14528BCP	16			8
7	DM74LS10N			14	7
8	N74LS00N			14	7
9	MC14066BCP				7
10	MC14503BCP	16			8
11	MC14071BCP	14			7
12	MC14011CP	14			7
13	74H102			7	14
14	74H102			7	14
15	MC14011CP	14			7
16	MC14073BCP	14			7
17	CD4095BE	14			7
18	CD4510BCN	16			8
19	SN74LS19ON			16	8
20	N74LS74N883C		14		7

MICROCIRCUIT INFORMATION

U NO	TYPE	POWER (V DC) +5V (5)	+5	+5 (FLTR)	GND
21	MC14081BCP	14			7
22	F4049BCP	1			8
23	CD4510BCN	16			8
24	SN74LS19ON		16		8
25	N74LS00N		14		7
26	CD4510BCN	16			8
27	SN74LS19ON		16		8
28	N74LS74N883C		14		7
29	MC14066BCP				7
30	MC14503BCP	16			8
31	SN74LS19ON		16		8
32	SN74LS19ON		16		8
33	SN74LS19ON		16		8
34	DM74LS10N		14		7
35	MC14503BCP	16			8
36	(3)				
37	LM317T	SEE	DRG		
38	SN74LS193N		16		8
39	SN74LS19ON		16		8
40	MC14011CP		14		7

NOTES;

1. UNLESS OTHERWISE SPECIFIED ALL RESISTENCE VALUES ARE IN OHMS, ALL CAPACITANCE VALUES ARE IN MICROFARADS, ALL INDUCTANCE VALUES ARE IN MICROHENRYS AND ALL DIODES ARE 1N4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. U36 IS A 220 k RESISTOR ARRAY

U36

4. BY-PASS CAPACITORS DISTRIBUTED THROUGHOUT BOARD.
5. +5 V IS A KEEP ALIVE VOLTAGE.

634-6687

VBFO, Schematic Diagram
Figure 6 (Sheet 4)